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09/166,488	10/05/1998	GREGORY F. BECK	36J.P164	9206

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FITZPATRICK CELLA HARPER & SCINTO
30 ROCKEFELLER PLAZA
NEW YORK, NY 10112

EXAMINER	
KING, JUSTIN	

ART UNIT	PAPER NUMBER
2111	19

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/166,488	BECK ET AL.	
	Examin r	Art Unit	
	Justin I. King	2111	

-- The MAILING DATE of this communication appears on the cover she t with th correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 September 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19 and 24-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19 and 24-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *18* .
4) ☐ Interview Summary (PTO-413) Paper No(s). ___ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1-4, 10-13, 19, 24-26, and 32-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of the Stancil (U.S. Patent No. 5,963,431),"Packet: header and data" from the Technische University's Distributed system class, and "CP/IP abc's" by TechEncyclopedia.

Referring to claim 1: Stancil discloses a system with a first interface (column 3, lines 7-8) and a second interface (column 3, line 13) and a controller (figure 1, structure 16, CPU). Stancil discloses and teaches that it is known to equip two IEEE 1394 controller interfaces; furthermore, court has held that duplication of the essential working parts involves only routine skill in the art (MPEP 2144, St. Regis Paper Co. v. Bemis Co., 193 USPQ 8), therefore, to equip additional IEEE 1394 controller interface will only involves routine skills in the art. Stancil does

not explicitly disclose detailed data packet practice. TechEncyclopedia discloses a commonly practicing OSI seven-layer model for data transmission, and the Technische University' class note teaches that it is known to package each packet with a header and forward it; Technische University further discloses the possible header contents include source and destination address, which is containing information about the data. Thus, it discloses the receiving data from the bus, attaching an identification (ID) header to the received data, and retransmitting the received data with the ID header onto the bus, and receiving data with the ID header attached thereto, interpreting the ID header to identify which of the first or second interfaces should receive the data, and transmitting the data over the bus to the identified interface.

Both Stancil's 1394-interface controllers has to connect to an internal motherboard bus for data transmitting, such as an industrial well-known PCI bus. Since the data is transmitted between two separate protocols, the 1394 protocol and the internal bus protocol, the internal bus will translate any received 1394 packets into its own format, which it will attach an ID header is other than a 1394 header formatted in IEEE 1394 standard and contains information about the data according to the OSI model and Technische University's teaching. Since the header information contains the designation, the 1394 interface will generate its 1394 header with the designation it receives from the internal bus' data packet's header; hence, the 1394 header is built based on information contained in the ID header.

Hence, it would have been obvious to one having ordinary skill in the computer art to combine Stancil, OSI model, and packet switching because both OSI model and packet switching are common industrial practices, and adding any additional interface controller to the system only involves routine skill in the art.

Referring to claim 2: Claim 1's rejection applies; furthermore, as the specification states, it is known the digital video camera having a fixed broadcast channel for transmitting/receiving digital video data isochronously on a 1394 bus. It is a designer's choice to select digital cameras as the 1394 device connecting to the 1394 bus. The selection of the type of 1394 devices is inconsequential for the invention as a whole and presents no new or unexpected result, so long as the data is successfully transmitted on the same broadcast channel. Therefore, the selection of particular type of 1394 devices is a designer's choice.

Referring to claim 3: Claim 1's argument applies; furthermore, the Technische teaches that the ID header identifies the type of data, the data recipient and amount of data.

Referring to claim 4: Claims 1 and 2's arguments apply; furthermore, the 1394 header is part of IEEE 1394 standard; and the OSI seven-layer model discloses that a link layer for each respective interface removes the header and header check and data check information prior to transmitting the data.

Referring to claim 10: Claim 1's argument applies; furthermore, the PCI bus is a designer choice. Each computer system has to have at least one internal bus, the selection of the internal bus protocol is inconsequential for the invention as a whole and presents no new or unexpected results, so long as the internal bus is capable to transmit the required data successfully. In addition, the PCI is a well-known industrial practice.

Referring to claim 11: Stancil discloses a system with a first interface (column 3, lines 7-8) and a second interface (column 3, line 13) and a controller (figure 1, structure 16, CPU). Stancil discloses and teaches that it is known to equip two IEEE 1394 controller interfaces; furthermore, court has held that duplication of the essential working parts involves only routine

skill in the art (MPEP 2144, St. Regis Paper Co. v. Bemis Co., 193 USPQ 8), therefore, to equip additional IEEE 1394 controller interface will only involves routine skills in the art. Stancil does not explicitly disclose detailed data packet practice. TechEncyclopedia discloses a commonly practicing OSI seven-layer model for data transmission, and the Technische University' class note teaches that it is known to package each packet with a header and forward it; Technische University further discloses the possible header contents include source and destination address, which is containing information about the data. Thus, it discloses the receiving data from the bus, attaching an identification (ID) header to the received data, and retransmitting the received data with the ID header onto the bus, and receiving data with the ID header attached thereto, interpreting the ID header to identify which of the first or second interfaces should receive the data, and transmitting the data over the bus to the identified interface.

Both Stancil's 1394-interface controllers has to connect to an internal motherboard bus for data transmitting, such as an industrial well-known PCI bus. Since the data is transmitted between two separate protocols, the 1394 protocol and the internal bus protocol, the internal bus will translate any received 1394 packets into its own format, which it will attach an ID header is other than a 1394 header formatted in IEEE 1394 standard and contains information about the data according to the OSI model and Technische University's teaching. Since the header information contains the designation, the 1394 interface will generate its 1394 header with the designation it receives from the internal bus' data packet's header; hence, the 1394 header is built based on information contained in the ID header.

Hence, it would have been obvious to one having ordinary skill in the computer art to combine Stancil, OSI model, and packet switching because both OSI model and packet

switching are common industrial practices, and adding any additional interface controller to the system only involves routine skill in the art.

Referring to claim 12: Claim 11's argument applies; furthermore, claim 12 is rejected with claim 2's argument.

Referring to claim 13: Claims 11 and 12's arguments apply; furthermore, claim 13 is rejected with claim 4's argument, and the CPU is well-known in packet switching operations.

Referring to claim 19: Claim 11's argument applies; furthermore, claim 19 is rejected with claim 10's argument.

Referring to claim 24: Stancil discloses a system with a first interface (column 3, lines 7-8) and a second interface (column 3, line 13) and a controller (figure 1, structure 16, CPU). Stancil discloses and teaches that it is known to equip two IEEE 1394 controller interfaces; furthermore, court has held that duplication of the essential working parts involves only routine skill in the art (MPEP 2144, St. Regis Paper Co. v. Bemis Co., 193 USPQ 8), therefore, to equip additional IEEE 1394 controller interface will only involves routine skills in the art. Stancil does not explicitly disclose detailed data packet practice. TechEncyclopedia discloses a commonly practicing OSI seven-layer model for data transmission, and the Technische University' class note teaches that it is known to package each packet with a header and forward it; Technische University further discloses the possible header contents include source and destination address, which is containing information about the data. Thus, it discloses the receiving data from the bus, attaching an identification (ID) header to the received data, and retransmitting the received data with the ID header onto the bus, and receiving data with the ID header attached thereto,

interpreting the ID header to identify which of the first or second interfaces should receive the data, and transmitting the data over the bus to the identified interface.

Both Stancil's 1394-interface controllers has to connect to an internal motherboard bus for data transmitting, such as an industrial well-known PCI bus. Since the data is transmitted between two separate protocols, the 1394 protocol and the internal bus protocol, the internal bus will translate any received 1394 packets into its own format, which it will attach an ID header is other than a 1394 header formatted in IEEE 1394 standard and contains information about the data according to the OSI model and Technische University's teaching. Since the header information contains the designation, the 1394 interface will generate its 1394 header with the designation it receives from the internal bus' data packet's header; hence, the 1394 header is built based on information contained in the ID header.

Hence, it would have been obvious to one having ordinary skill in the computer art to combine Stancil, OSI model, and packet switching because both OSI model and packet switching are common industrial practices, and adding any additional interface controller to the system only involves routine skill in the art.

Referring to claim 25: Claim 24's argument applies; furthermore, claim 25 is rejected with claim 2's argument.

Referring to claim 26: Claims 24-25's arguments apply; furthermore, claim 26 is rejected with claim 4's argument.

Referring to claim 32: Claim 24's argument applies; furthermore, claim 32 is rejected with claim 10's argument.

Referring to claim 33: Stancil discloses a system with a first interface (column 3, lines 7-8) and a second interface (column 3, line 13) and a controller (figure 1, structure 16, CPU). Stancil discloses and teaches that it is known to equip two IEEE 1394 controller interfaces; furthermore, court has held that duplication of the essential working parts involves only routine skill in the art (MPEP 2144, St. Regis Paper Co. v. Bemis Co., 193 USPQ 8), therefore, to equip additional IEEE 1394 controller interface will only involves routine skills in the art. Stancil does not explicitly disclose detailed data packet practice. TechEncyclopedia discloses a commonly practicing OSI seven-layer model for data transmission, and the Technische University' class note teaches that it is known to package each packet with a header and forward it; Technische University further discloses the possible header contents include source and destination address, which is containing information about the data. Thus, it discloses the receiving data from the bus, attaching an identification (ID) header to the received data, and retransmitting the received data with the ID header onto the bus, and receiving data with the ID header attached thereto, interpreting the ID header to identify which of the first or second interfaces should receive the data, and transmitting the data over the bus to the identified interface.

Both Stancil's 1394-interface controllers has to connect to an internal motherboard bus for data transmitting, such as an industrial well-known PCI bus. Since the data is transmitted between two separate protocols, the 1394 protocol and the internal bus protocol, the internal bus will translate any received 1394 packets into its own format, which it will attach an ID header is other than a 1394 header formatted in IEEE 1394 standard and contains information about the data according to the OSI model and Technische University's teaching. Since the header information contains the designation, the 1394 interface will generate its 1394 header with the

designation it receives from the internal bus' data packet's header; hence, the 1394 header is built based on information contained in the ID header.

Hence, it would have been obvious to one having ordinary skill in the computer art to combine Stancil, OSI model, and packet switching because both OSI model and packet switching are common industrial practices, and adding any additional interface controller to the system only involves routine skill in the art.

Referring to claim 34: Stancil discloses a system with a first interface (column 3, lines 7-8) and a second interface (column 3, line 13) and a controller (figure 1, structure 16, CPU). Stancil discloses and teaches that it is known to equip two IEEE 1394 controller interfaces; furthermore, court has held that duplication of the essential working parts involves only routine skill in the art (MPEP 2144, St. Regis Paper Co. v. Bemis Co., 193 USPQ 8), therefore, to equip additional IEEE 1394 controller interface will only involves routine skills in the art. Stancil does not explicitly disclose detailed data packet practice. TechEncyclopedia discloses a commonly practicing OSI seven-layer model for data transmission, and the Technische University' class note teaches that it is known to package each packet with a header and forward it; Technische University further discloses the possible header contents include source and destination address, which is containing information about the data. Thus, it discloses the receiving data from the bus, attaching an identification (ID) header to the received data, and retransmitting the received data with the ID header onto the bus, and receiving data with the ID header attached thereto, interpreting the ID header to identify which of the first or second interfaces should receive the data, and transmitting the data over the bus to the identified interface.

Both Stancil's 1394-interface controllers has to connect to an internal motherboard bus for data transmitting, such as an industrial well-known PCI bus. Since the data is transmitted between two separate protocols, the 1394 protocol and the internal bus protocol, the internal bus will translate any received 1394 packets into its own format, which it will attach an ID header is other than a 1394 header formatted in IEEE 1394 standard and contains information about the data according to the OSI model and Technische University's teaching. Since the header information contains the designation, the 1394 interface will generate its 1394 header with the designation it receives from the internal bus' data packet's header; hence, the 1394 header is built based on information contained in the ID header.

Hence, it would have been obvious to one having ordinary skill in the computer art to combine Stancil, OSI model, and packet switching because both OSI model and packet switching are common industrial practices, and adding any additional interface controller to the system only involves routine skill in the art.

Referring to claim 35: Stancil discloses a system with a first interface (column 3, lines 7-8) and a second interface (column 3, line 13) and a controller (figure 1, structure 16, CPU). Stancil discloses and teaches that it is known to equip two IEEE 1394 controller interfaces; furthermore, court has held that duplication of the essential working parts involves only routine skill in the art (MPEP 2144, St. Regis Paper Co. v. Bemis Co., 193 USPQ 8), therefore, to equip additional IEEE 1394 controller interface will only involves routine skills in the art. Stancil does not explicitly disclose detailed data packet practice. TechEncyclopedia discloses a commonly practicing OSI seven-layer model for data transmission, and the Technische University' class note teaches that it is known to package each packet with a header and forward it; Technische

University further discloses the possible header contents include source and destination address, which is containing information about the data. Thus, it discloses the receiving data from the bus, attaching an identification (ID) header to the received data, and retransmitting the received data with the ID header onto the bus, and receiving data with the ID header attached thereto, interpreting the ID header to identify which of the first or second interfaces should receive the data, and transmitting the data over the bus to the identified interface.

Both Stancil's 1394-interface controllers has to connect to an internal motherboard bus for data transmitting, such as an industrial well-known PCI bus. Since the data is transmitted between two separate protocols, the 1394 protocol and the internal bus protocol, the internal bus will translate any received 1394 packets into its own format, which it will attach an ID header is other than a 1394 header formatted in IEEE 1394 standard and contains information about the data according to the OSI model and Technische University's teaching. Since the header information contains the designation, the 1394 interface will generate its 1394 header with the designation it receives from the internal bus' data packet's header; hence, the 1394 header is built based on information contained in the ID header.

Hence, it would have been obvious to one having ordinary skill in the computer art to combine Stancil, OSI model, and packet switching because both OSI model and packet switching are common industrial practices, and adding any additional interface controller to the system only involves routine skill in the art.

Referring to claim 36: Stancil discloses a system with a first interface (column 3, lines 7-8) and a second interface (column 3, line 13) and a controller (figure 1, structure 16, CPU). Stancil discloses and teaches that it is known to equip two IEEE 1394 controller interfaces;

furthermore, court has held that duplication of the essential working parts involves only routine skill in the art (MPEP 2144, St. Regis Paper Co. v. Bemis Co., 193 USPQ 8), therefore, to equip additional IEEE 1394 controller interface will only involves routine skills in the art. Stancil does not explicitly disclose detailed data packet practice. TechEncyclopedia discloses a commonly practicing OSI seven-layer model for data transmission, and the Technische University' class note teaches that it is known to package each packet with a header and forward it; Technische University further discloses the possible header contents include source and destination address, which is containing information about the data. Thus, it discloses the receiving data from the bus, attaching an identification (ID) header to the received data, and retransmitting the received data with the ID header onto the bus, and receiving data with the ID header attached thereto, interpreting the ID header to identify which of the first or second interfaces should receive the data, and transmitting the data over the bus to the identified interface.

Both Stancil's 1394-interface controllers has to connect to an internal motherboard bus for data transmitting, such as an industrial well-known PCI bus. Since the data is transmitted between two separate protocols, the 1394 protocol and the internal bus protocol, the internal bus will translate any received 1394 packets into its own format, which it will attach an ID header is other than a 1394 header formatted in IEEE 1394 standard and contains information about the data according to the OSI model and Technische University's teaching. Since the header information contains the designation, the 1394 interface will generate its 1394 header with the designation it receives from the internal bus' data packet's header; hence, the 1394 header is built based on information contained in the ID header.

Hence, it would have been obvious to one having ordinary skill in the computer art to combine Stancil, OSI model, and packet switching because both OSI model and packet switching are common industrial practices, and adding any additional interface controller to the system only involves routine skill in the art.

Referring to claim 37: Stancil discloses a system with a first interface (column 3, lines 7-8) and a second interface (column 3, line 13) and a controller (figure 1, structure 16, CPU). Stancil discloses and teaches that it is known to equip two IEEE 1394 controller interfaces; furthermore, court has held that duplication of the essential working parts involves only routine skill in the art (MPEP 2144, St. Regis Paper Co. v. Bemis Co., 193 USPQ 8), therefore, to equip additional IEEE 1394 controller interface will only involves routine skills in the art. Stancil does not explicitly disclose detailed data packet practice. TechEncyclopedia discloses a commonly practicing OSI seven-layer model for data transmission, and the Technische University' class note teaches that it is known to package each packet with a header and forward it; Technische University further discloses the possible header contents include source and destination address, which is containing information about the data. Thus, it discloses the receiving data from the bus, attaching an identification (ID) header to the received data, and retransmitting the received data with the ID header onto the bus, and receiving data with the ID header attached thereto, interpreting the ID header to identify which of the first or second interfaces should receive the data, and transmitting the data over the bus to the identified interface.

Both Stancil's 1394-interface controllers has to connect to an internal motherboard bus for data transmitting, such as an industrial well-known PCI bus. Since the data is transmitted between two separate protocols, the 1394 protocol and the internal bus protocol, the internal bus

will translate any received 1394 packets into its own format, which it will attach an ID header is other than a 1394 header formatted in IEEE 1394 standard and contains information about the data according to the OSI model and Technische University's teaching. Since the header information contains the designation, the 1394 interface will generate its 1394 header with the designation it receives from the internal bus' data packet's header; hence, the 1394 header is built based on information contained in the ID header.

Hence, it would have been obvious to one having ordinary skill in the computer art to combine Stancil, OSI model, and packet switching because both OSI model and packet switching are common industrial practices, and adding any additional interface controller to the system only involves routine skill in the art.

Referring to claim 38: Stancil discloses a system with a first interface (column 3, lines 7-8) and a second interface (column 3, line 13) and a controller (figure 1, structure 16, CPU). Stancil discloses and teaches that it is known to equip two IEEE 1394 controller interfaces; furthermore, court has held that duplication of the essential working parts involves only routine skill in the art (MPEP 2144, St. Regis Paper Co. v. Bemis Co., 193 USPQ 8), therefore, to equip additional IEEE 1394 controller interface will only involves routine skills in the art. Stancil does not explicitly disclose detailed data packet practice. TechEncyclopedia discloses a commonly practicing OSI seven-layer model for data transmission, and the Technische University' class note teaches that it is known to package each packet with a header and forward it; Technische University further discloses the possible header contents include source and destination address, which is containing information about the data. Thus, it discloses the receiving data from the bus, attaching an identification (ID) header to the received data, and retransmitting the received

data with the ID header onto the bus, and receiving data with the ID header attached thereto, interpreting the ID header to identify which of the first or second interfaces should receive the data, and transmitting the data over the bus to the identified interface.

Both Stancil's 1394-interface controllers has to connect to an internal motherboard bus for data transmitting, such as an industrial well-known PCI bus. Since the data is transmitted between two separate protocols, the 1394 protocol and the internal bus protocol, the internal bus will translate any received 1394 packets into its own format, which it will attach an ID header is other than a 1394 header formatted in IEEE 1394 standard and contains information about the data according to the OSI model and Technische University's teaching. Since the header information contains the designation, the 1394 interface will generate its 1394 header with the designation it receives from the internal bus' data packet's header; hence, the 1394 header is built based on information contained in the ID header.

Hence, it would have been obvious to one having ordinary skill in the computer art to combine Stancil, OSI model, and packet switching because both OSI model and packet switching are common industrial practices, and adding any additional interface controller to the system only involves routine skill in the art.

4. Claims 5-9, 14-18, and 27-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of the Stancil, "Packet: header and data" from the Technische University's Distributed system class, "CP/IP abc's" by TechEncyclopedia, and "IEEE 1394 The Cable Connection to Complete The Digital Revolution" by Daniel Moore.

Referring to claims 5-7: Claims 1 and 2's arguments apply; furthermore, Moore discloses that it is known to connect 1394 nodes with a network controller for accessing a local area network and for transmitting data. As Stated above, the OSI seven-layer and Technische University disclose the packet switching practice, which also applies to the network packets, such that the network controller receives the data and the ID header, attaches a network header to the data and repackages the data with the ID header and network header into a network data packet and, upon receiving access to the local area network, transmits the network packet over the local area network to a receiving side network controller based on the attached network header, and the wherein received network data packets are unpackaged, network headers are removed, and the ID header is interpreted to identify which interface should receive the data.

Referring to claim 8: Claims 1-2 and 5-7's arguments apply; furthermore, it is a common practice to equip a monitor for displaying analog video data output from either the first or second digital video camera.

Referring to claim 9: Claim 1's argument applies; furthermore, claim 9 is rejected with claim 5's argument stated above.

Referring to claims 14-16: Claims 11 and 12's arguments apply; furthermore, claim 14 is rejected with claims 5-7's arguments.

Referring to claim 17: Claims 11-12 and 14-16's arguments applies; furthermore, it is a common practice to equip a monitor for displaying digital video data output from either the first or second digital video camera.

Referring to claim 18: Claim 11's argument applies; furthermore, claim 18 is rejected with the claim 14's argument.

Referring to claims 27-29: Claims 24-25's arguments apply; furthermore, claim 27 is rejected with claims 5-7's arguments and the channel information is part of IEEE 1394 standard.

Referring to claim 30: Claims 24-25 and 27-29's arguments apply; furthermore, it is a common practice to equip a monitor for displaying analog video data output from either the first or second digital video camera.

Referring to claim 31: Claim 24's argument applies; furthermore, claim 31 is rejected with the claim 27's rejection.

Response to Arguments

5. In response to Applicant's argument that prior arts do not teach or suggest interpreting an ID header to determine which of a first and second interface should received the data, and using the ID header, which is other than a 1394 header, to build the 1394 based on information contained in the ID header (Remark, page 19, paragraph 3): The header attaching and removing are part of the TCP/IP OSI seven-layer model practice. The prior art discloses PCI and 1394. PCI and 1394 are two different buses; therefore, any PCI packet designated to a 1394 device will be re-packaged in 1394 standard, and thus it is using the PCI ID header, which is other than a 1394 header, to build a 1394 header. Since the prior art teaches it is known to equip more than one 1394 interface controller, the computer system controls access each device on each 1394, thus the system directs the PCI packets to its designated 1394 controller/device.

Conclusion

6. The prior art made of recorded and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 5,963,431 to Stancil: Stancil discloses that it is a common practice to equip two 1394 interfaces in one system.

U.S. Patent No. 5,161,857 to Mayercheck et al.: Mayercheck discloses that it is known that the camera can have either digital or analogy output.

U.S. Patent No. 5,754,548 to Hoekstra et al.: Hoekstra discloses an interconnection of local communication bus system.

U.S. Patent No. 6,480,889 to Saito et al.: Saito discloses a scheme for managing nodes connected to a home network according to their physical location.

U.S. Patent No. 5,634,010 to Ciscon et al.: Ciscon discloses a method of managing and distributing data objects of different types between computers connected to a network.

U.S. Patent No. 5,383,187 to Vardakas et al.: Vardakas discloses an adaptive protocol for packet communications network and method.

U.S. Patent No. 5,442,630 to Gagliardi et al.: Gagliardi discloses an ISDN interfacing for local area network.

U.S. Patent No. 5,937,175 to Sescila, III et al.: Sescila discloses a translator from the PCI bus to the IEEE 1394 bus. Sescila teaches that it is known to translate data between PCI and 1394.

U.S. Patent No. 6,211,800 to Yanagihara et al.: Yanagihara discloses a data decoding system and method to transfer device and receiving device for MPEG program stream.

U.S. Patent No. 6,219,697 to Lawande et al.: Lawande discloses a method and apparatus for operating the Internet protocol over a hight-speed serial bus.

U.S. Patent No. 5,335,325 to Frankl et al.: Frank discloses that the CPU is known in the packet switching operations.

U.S. Patent No. 4,742,511 to Johnson, Douglas A.: Johnson discloses that the CPU is known in the packet switching operations.

"IEEE Standard for a High Performance Serial Bus" by IEEE Computer Society: The IEEE standard discloses that 1394's data packet format and teaches that the closed loop is not supported.

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a)..

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Justin King whose telephone number is (703) 305-4571. The examiner can normally be reached on Monday through Friday from 9:00 A.M. to 5:00 P.M..

If attempts to reach the examiner by telephones are unsuccessfully, the examiner's supervisor, Mark Reinhart can be reached at (703) 308-3110.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose number is (703)-306-5631.

Justin King
January 22, 2004

XUAN M. THAI
PRIMARY EXAMINER
TC 2100